ESF Exploratory Workshop on

"Silicon/oxide hetero-epitaxy: a new road towards a Si-CMOS-compatible resonant tunnel diode technology?"

SCIENTIFIC REPORT

September 11 – 13th, 2006
Villa Olmo, Como, Italy

Workshop Convenors:
Gerd Norga, Politecnico di Milano
Igor Zozoulenko, University of Linköping

1. Executive Summary

On September 11-12th, 2006, an ESF Exploratory workshop on "*Silicon/oxide hetero-epitaxy: a new road towards a Si-CMOS-compatible resonant tunnel diode technology*" was held in Villa Olmo, on the banks of Lake Como. The workshop brought together MBE growers, advanced characterization specialists, and resonant tunneling diode (RTD) physics experts to discuss recent advances in the theory and practice of silicon-compatible RTDs. An important emphasis was placed on RTDs based on crystalline silicon/oxide hetero-interfaces, grown by molecular beam epitaxy (MBE).

Semiconductor researchers have known since the 1950s that the quantum-confinement effects in a thin semiconductor well sandwiched between two higher bandgap materials result in an N-shaped (I,V) characteristic. The resulting "resonant tunnel diode" (RTD) exhibits negative differential resistance (NDR). Circuit designers realized early on that the NDR functionality of RTDs, in combination with transistors, can boost circuit speed while reducing component count and power consumption. Processing difficulties so far precluded the growth of high quality epitaxial insulator/Si/insulator structures, confining tunnel diodes to exotic III-V semiconducting materials. Recently however, the interest in silicon-based RTDs has risen dramatically because the combination of oxide/silicon/oxide RTDs and silicon MOSFETs could overcome limits to performance scaling of silicon CMOS (the so called "red brick wall" marking the end of Moore's Law).

The main aim of the ESF workshop on "Silicon/oxide hetero-epitaxy: a new road towards a Si-CMOS-compatible resonant tunnel diode technology" was to bring together several groups in Europe which are currently performing research on the topic of Si-compatible RTDs, either emphasizing technology/circuit modeling, device modeling using quantum physics, or layer growth. Because the development of a high-performance Si-based RTD technology will requires a concerted, multidisciplinary effort from materials growers, characterization, and device physics and circuit modeling experts, there is a strong need for the respective communities to join forces. The workshop provided an opportunity for crossdisciplinary networking, to help consolidate

ongoing efforts to define a multidisciplinary consortium which could jointly apply for EU funding, for instance as a STREP consortium under the 7th Framework Program.

The ESF Exploratory workshop consisted of 11 invited talks (40 minutes presentation + 10 minutes discussion), divided over 4 sessions (1. RTD – CMOS Co-integration: state of the art; 2. Si/Oxide Hetero-Epitaxy I; 3. Silicon/Oxide Hetero-epitaxy II; 4.RTD Device Theory and Modeling). There was one additional session about EU Funding Opportunities with a presentation by a member of the Politecnico di Milano's Technology Transfer Office (Dr. Suevo), followed by a roundtable discussion chaired by the workshop convenors. During the coffee breaks, a poster session was held to give the more junior participants an occasion to present their research work.

Based on the feedback received from many participants during and after the meeting, the main factor for the workshop's success was found to be the high quality of the invited speakers (score 4.33 / 5 for technical quality, where 4 = very good and 5 = excellent) and the high quality of the organization (score 4.11/5 for general organization). The presentations were well structured, and all speakers devoted a part of their time to a tutorial part to take into account the multidisciplinary audience. Most presentations were followed by a lively discussion of high scientific level, helped by the relaxed, collegial atmosphere and the relatively small size of the audience.

2. Scientific content of the event

The first session (RTD-CMOS co-integration: state of the art) was opened by **Paul Berger** (Ohio State University) who presented an overview presentation of the results obtained by his research group and collaborators in the field of resonant interband tunneling diodes (RITD) starting in the late 1990s. Their technology is based on an advanced low temperature molecular beam epitaxy process (LTMBE), combined with delta doping to introduce a 2 dimensional electron gas on either side of the junction. This technology resulted in a peak valley current ratio (PVCR) at room temperature of 4, and a peak current tunable from 20 mA/cm^2 to 150 kA/cm^2 by varying the tunnel barrier

thickness. Monolithic integration with CMOS and multivalue logic implementation have also been demonstrated. The presentation of **M. Mouis** (IMEP-CNRS, Grenoble) first presented an overview of the state of the art in III-V RTDs, pointing out that power limitations are the main show stopper for analogue applications of RTD devices, whereas for digital application the difficulty of integrating III-V and logic functions remains an issue. Si-based RTDs would represent an interesting alternative because their integration with CMOS should at least in principle be more straightforward. The most interesting system are Si/oxide based RTD's because of the superior band offsets obtainable compared to SiGe based RTDs, which result in larger peak valley current ratios. Simulations were presented for Si based RTD devices with SiO_2 and HfO_2 barriers. HfO_2 is predicted to outperform SiO_2, however there is a need to select low effective mass carriers, which can be achieved by lateral confinement or by strain engineering as used for mobility enhancement in CMOS. Finally it was pointed out that, although double gated devices and RTDs feature a similar layout, the oxide thicknesses required for RTDs would necessitate the fabrication of RTD and double gated devices in separate fabrication steps. **Douglas Paul** (University of Cambridge) presented his research group's contributions to the field of resonant intraband tunneling diodes (RTD). This technology makes use of the commensurate growth of SiGe on relaxed SiGe buffers. A Si well under tensile stress, and a Ge rich barrier under compressive stress results in suitable bandoffsets between the Si well and the SiGe barriers. The system is a natural candidate for integration with strained Si CMOS transistors. Because of the high thermal budget needed for CMOS implant anneals, the RTD are integrated after the strained CMOS front end process, which requires selective SiGe CVD growth within oxide windows.

M. Stoffel (Max-Planck Institute for Solid State Research, Stuttgart) presented his work on Si and SiGe based resonant interband tunneling diodes (RITD). Interesting results included the observation of light emission from Si based interband tunneling diodes, and the first observation of negative differential resistance in Ge quantum dot based diodes.

In the second and third sessions (Silicon/oxide hetero-epitaxy I and II) and overview was given on epitaxial growth techniques (mostly MBE based) for the growth of single crystalline tunnel barriers on Si and vice versa (i.e. Si re-epitaxy on a single crystalline insulator layer). **J. W. Seo** (EPF Lausanne) presented an overview of high resolution

transmission electron microscopy studies of $SrTiO_3$/Si, $LaZrO_3$/Si and graded $SrHfO_3$/$SrZrO_3$/Si. This presentation demonstrated that the growth of "device quality" Si and Ge overlayers is still a challenge, and the exact mechanism of mismatch accommodation in the presence an amorphous SiO_2 interfacial layers remains to be clarified. **A. Dimoulas** (National Center for Scientific Research "Demokritos", Athens) presented his group's work on the use of $(La,Y)_2O_3$ templates. These bixbyite films can be used to obtain Si(110) oriented epilayers starting from a Si(100) substrate. The appearance of 2 different domains (110) (related to the steps on the Si(100) surface) can be surpressed by using Si(100) wafers with a large miscut (featuring double steps). Next, the results of Ge overgrowth on Si were presented using $SrHfO_3$ template layers (work carried out in collaboration with IBM Zurich Research Laboratory). A high-low-high temperature process was presented which results in Ge epilayers with quite low defect content as evident from TEM. However, the rather large thicknesses (several 100 nm) necessary to obtain films of high structural quality preclude the use of this approach for RTD applications.

The presentation of **J. Osten** (U. Hannover) focused on the Rare Earth oxides Gd_2O_3 and Pr_2O_3. In this system high quality epitaxy can be obtained on (111) oriented Si substrates. Islanding (due to the so-called "Murphy's law of epitaxy") can be suppressed using "encapsulated solid-phase epitaxy" (deposition of semi-amorphous oxide on top of amorphous Si, prior to recrystallization of the full stack at high temperature in UHV). While the precise mechanism of this technique remains poorly understood, the resulting epitaxial quality for a Si/Gd_2O_3/Si/Gd_2O_3 stack (HRTEM images) was rather impressive.

The talk by **G. Hollinger** (CNRS-LEOM) and the posters by his collaborators (**G. Saint-Girons, M. Beccera, C. Merckling**) covered epitaxy of $SrTiO_3$, γ-Al_2O_3 and $LaAlO_3$ on Si. Notwithstanding the large mismatch in the γ-Al_2O_3 on Si system, high quality epilayers can be obtained on Si(111). In Si (100), γ-Al_2O_3 grows initially commensurately (up to a thickness of 1 nm), but then converts to (111) orientation.

M. Ishida (Toyohashi University of Technology, Japan) presented further results on the γ-Al_2O_3 on Si system (both grown by chemical vapor deposition (CVD) and by MBE). This system has been studied both for use as gate dielectric for CMOS and as template for re-epitaxy of Si. High quality Si re-epitaxy on γ-Al_2O_3 is possible by first depositing a

layer of unoxidized Al prior to Si epitaxy. This layer increases the surface energy of the starting surface for Si epitaxy, facilitating smooth layer by layer growth. Finally, the scientific part of the workshop was concluded with two theory talks. “Simulation and modelling of RTD devices” by **I. Zozoulenko** (University of Linköping, Sweden) emphasized the potential of lateral scaling of RTD devices, while “Modelling of Quantum transport in Semiconductor Heterostructures and RTD Circuits” by **W. Mathis** (University of Hannover, Germany) discussed several interesting circuit concepts which incorporate nonlinear two-terminal circuit elements such as RTDs.

3. Final Workshop Program

Tuesday 12 September 2006

09.00 - 09.15 **Welcome and opening remarks / Presentation of the European Science Foundation (ESF)**

G. Norga *(Politecnico di Milano, Italy),* **I. Zozoulenko** *(Linköping University, Sweden)*
Workshop Convenors

09.15 – 09.30 **Research activities at L-NESS**
L. Miglio *(University of Milano-Bicocca, Italy), LNESS Director*

SESSION 1: RTD-CMOS CO-INTEGRATION: STATE OF THE ART

09.30 – 10.15 **Extending CMOS: Quantum Functional Circuits using Si-based Resonant Interband Tunnel Diodes**
P. Berger*, Ohio State University, USA*

10.15 – 10.45 *Coffee break*

10.45 – 11.30 **From III-V to Si-based RTDs**
M. Mouis *(IMEP-CNRS, Grenoble, France),* **O. Vanbésien** *(IEMNCNRS, Lille, France)*

11.30 – 12.15 **Integrating Si/SiGe RTDs with strained-Si CMOS transistors**
D. Paul *(Cavendish Laboratory, Cambridge University, UK)*

12.15 – 13.00 **Si/SiGe based interband tunneling diodes grown by MBE**
Mathieu Stoffel *(Max-Planck-Institut für Festkoerperforschung,Stuttgart, Germany)*

13.00 – 14.30 *Lunch*

SESSION 2: SI/OXIDE HETERO-EPITAXY I

14.30- 15.15 **Si/oxide interface: structural and chemical stability**
J. W. Seo *(Ecole Polytechniqe Fédérale de Lausanne, Switzerland)*

15.15 – 16.00 Si **and Ge overgrowth on epitaxial oxides**
A. Dimoulas *(National Center for Scientific Research "Demokritos",Athens, Greece)*

16.00 – 16.30 *Coffee break*

16.30 – 17.15 **MBE growth and Properties of Crystalline Oxide/Silicon/Oxide Nanostructures**
J. Osten *(University of Hannover, Germany)*

17.30 – 18.30 *L-NESS Visit*

19.30 – 21.30 *Conference dinner*

Wednesday 13 September 2006

SESSION 3: SILICON/OXIDE HETERO-EPITAXY II

09.00 – 09.45 **Epitaxial growth of Al_2O_3, $SrTiO_3$ and $LaAlO_3$ for monolithic integration on silicon**
G. Hollinger*, CNRS-LEOM - Ecole Centrale de Lyon, France*

09.45 – 10.30 **Hetero- epitaxial growth of Al_2O_3/Si and device applications**
M. Ishida*, Toyohashi University of Technology, Toyohashi, Japan*

10.30 – 11.00 *Coffee break*

SESSION 4: RTD THEORY AND DEVICE MODELING

11.00 – 11.45 **Simulation and modelling of RTD devices**
I. Zozoulenko*, University of Linköping, Sweden*

11.45 – 12.30 **Modelling of Quantum transport in Semiconductor Heterostructures and RTD Circuits**
W. Mathis*, University of Hannover, Germany*

12.30 – 14.00 *Lunch*

Session 5: FP 7 Funding opportunities
14.00 – 14.45 **Funding opportunities in the 7th Framework Program**

Stefania Suevo*, Politecnico di Milano, Italy*

14.45 – 15.30 **Roundtable with all interested participants**

15.30 – 16.00 *Coffee break*

16.00 – 17.00 **Workshop wrap-up**
G. Norga *(Politecnico di Milano, Italy),* **I. Zozoulenko** *(Linköping University, Sweden)*

Poster Session

1) L. Becerra[1], C. Merckling[1,2], Mario El-Kazzi[1], G. Saint-Girons[1], A. Poncet[3], L. Militaru[3], C. Plossu[3], P. Rojo Romeo[1], G. Hollinger[1] "**Resonant Tunneling Diode Al_2O_3 / Si / Al_2O_3**", [1] *LEOM – UMR CNRS 5512 – Ecole centrale de Lyon – 36 Avenue Guy de Collongue 69134 Ecully cedex, France,* [2] *STMicroelectronics – 850 Rue Jean Monnet 38926 Crolles, France,* [3] *LPM – UMR CNRS 5511 – INSA de Lyon – 7 Avenue Jean Capelle 69621 Villeurbanne cedex, France*

2) G. Delhaye[1], G. Saint-Girons[1], L. Largeau[3], G. Patriarche[3], C. Merckling[1,2], M. El Kazzi[1], M.Gendry[1], G. Hollinger[1], Y. Robach[1], "**Heteroepitaxial growth of SrTiO3 on Si(001) by molecular beam epitaxy**" (1) *LEOM (UMR CNRS 5512), École Centrale de Lyon, 69134 ECULLY Cedex – France* (2) *ST Microelectronics, 850 rue Jean Monnet, 38926 CROLLES – France*, (*3) LPN (UPR20/CNRS), route de Nozay 91460 Marcoussis-France.*

3) C. Merckling[1,2], M. El-Kazzi[1], G. Delhaye[1], S. Gaillard[2], L. Becerra[1], L. Rapenne[3], B. Chenevier[3], O. Marty[4], L. Largeau[5], G. Patriarche[5], G. Grenet[1], M. Gendry[1], Y. Robach[1], G. Saint-Girons[1], G. Hollinger[1], "**Epitaxial growth of γ-Al_2O_3 and $LaAlO_3$ on silicon**", *(1) LEOM - Ecole Centrale de Lyon, 36 avenue Guy de Collongue, 69134, Ecully, France, (2) ST Microelectronics, 850 rue Jean Monnet, 38926, Crolles, France (3) LMGP, 961 rue de la Houille Blanche, 38402, Saint Martin d'Hères, France (4) LENaC, 8 rue André-Marie Ampère, 69622, Villeurbanne, France (5) LPN - CNRS, Route de Nozay, 91460, Marcoussis, France*

4) A. Cattoni, R. Bertacco, M. Riva, M. Cantoni, F. Ciccacci, H. Von Känel and G.J. Norga, "**Effect of Ba termination layer on chemical and electrical passivation of Ge (100) surfaces**", *L-NESS, Dipartimento di Fisica, Politecnico di Milano, Via Anzani 42, I 22100 Italy*

5) "Alessandro Molle, Md. Nurul Kabir Bhuiyan, Grazia Tallarida, Marco Fanciulli", "**In situ UHV experiments on Ge substrates: from surface preparation to thin film growth and characterization**", *MDM-INFM Laboratory, CNR-INFM MDM National Laboratory, Via C. Olivetti 220041 Agrate Brianza (MI), Italy*.

4. Assessment of the results, contribution to the future direction of the field

The workshop represented 2 different communities which make up the RTD research community: one focused on the use of the SiGe system to realize the required bandoffsets, the other one interested in developing a viable technology for using silicon/oxide based RTDs. There are certain intrinsic advantages to the use of oxides (e.g. larger bandoffsets, therefore large peak to valley current ratios are attainable), but because of the limited epitaxial quality of the results obtained so far, this technology is quite immature in comparison with Si/Ge based RTDs.

Because of different levels of maturity of these two routes, the strategies for obtaining funding differ widely. In the late 90s quite some research, and also some European projects, were dedicated to basic epitaxial growth and device studies on SiGe RTD technology. To be fundable today, a project in this area should have a strong industrial flavor and focus to a greater extent on circuit and integration aspects. Meanwhile, the field of oxide/silicon hetero-epitaxy is rather young. Resonant Tunnel Diodes are just one of the many promising applications that this new technology platform has to offer, and realistic funding opportunities exist for a number of innovative epitaxial oxide-based devices. Some of the participants in the workshop were involved in EU projects that were submitted at the end of FP6 in the area of Si/oxide based RTDs. The reviewer's comments received for those proposals suggest that the speed advantage of RTD's is becoming a less convincing argument.

At the time of the conference, only scarce information was available about the funding priorities and call structure of FP7. The discussions at the roundtable therefore focused on suitable topics for future projects rather than on consortium building. A consensus was reached that the best strategy might be the preparation of a smaller, STREP-like project, probably not concentrating on RTD's alone, but considering RTDs alongside other novel devices enabled by epitaxial oxides technology.

After consultation with the participants, the organizers decided to publish all presentations in CD-ROM format. CDROMS were distributed to the workshop attendants as well as to the sponsors (ESF and Politecnico di Milano).

5. Statistical information on the participants

The convenors made a special effort to encourage the participation of young scientists; this effort was quite successful since of the people who finally attended the workshop, 45 % were in the $\leq$ 40 years age bracket (Figure 1).

The workshop attracted a total of 26 participants from 9 European countries, 1 from the USA and 1 from Japan (Figure 2). Growers (15) represented about 50 % of the audience, modeling experts (4) 15 % and characterization people (9) 35 %.

The gender breakdown was 25 % (7) female / 75 % male (21).

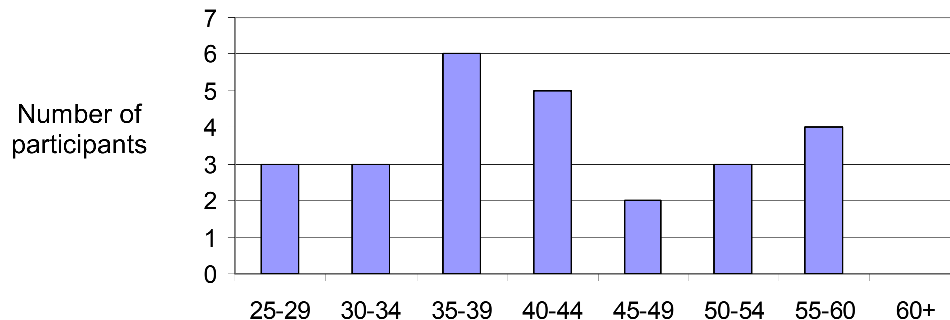

Figure 1: Age distribution of the participants.

Number of participants

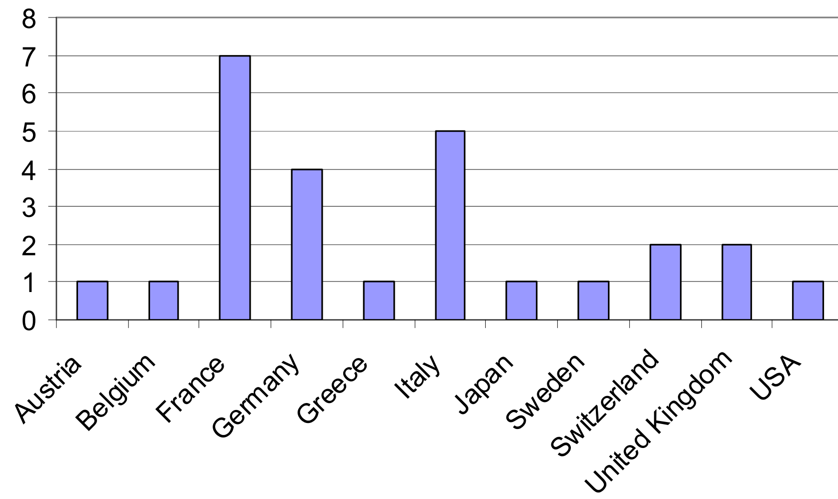

Figure 2: Geographical distribution of the participants.

6. Final List of Participants

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